No new matter is added.

Prior art rejection

Claims 1-8 were rejected under 35 USC §103(a) as being obvious over the admitted prior art (APA) in view of Morihisa (JP 10-173,070). It is believed that the claims will be seen to be patentably distinguished from the cited references in view of the following discussion.

The claimed invention pertains to an I/O protection circuit that uses field effect transistors (FETs). A conventional device is illustrate in Figure 7 of the application, where it is seen that the device includes an I/O input terminal 7 that is connected directly to the diffusion region 3b of an FET, and another diffusion 4a that is not part of the FET and that connects the substrate to a reference potential (in this case ground 9). One of Morihisa's devices is also discussed in the application at page 6 and is illustrated in Figure 11. Morihisa differs from the conventional device in that Morihisa provides a resistance element 13, 14 between the input terminal 7 and the drain 3b of the FET. Turning to the other embodiments disclosed in the Morihisa reference, the embodiment of Morihisa's Figure 2 utilizes a well 5' beneath the source of the FET as well as a resistance element 3, 17, 6.

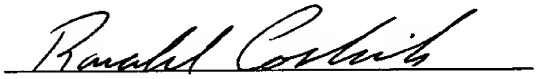
The claimed invention differs from the APA in that it uses a well beneath the source diffusion (see well 1a, Figure 2) that has a lower dopant concentration than the source diffusion. The official action notes that Morihisa also uses a well beneath the source diffusion in the embodiment of Morihisa's Figure 2. However, Morihisa does not teach using a well beneath a source diffusion in the absence of a resistance element between the input terminal and the drain. Morihisa teach the use of a resistance element (Figure 1a and 1b), and teaches the use of a well beneath the source diffusion ***in addition to*** a resistance element (Figure 2). However, the claimed invention specifies that a well is provided beneath the source and that an input terminal is connected ***directly*** to an FET drain ***with no intervening resistance element***. While Morihisa does use a well b neath the source, Morihisa teaches that this feature is used in conjunction with a resistive element between the input terminal and the drain. It

is therefore believed that one following Morihisa's teaching would implement both a resistive element ***and*** a well beneath the source, since to do otherwise would go against Morihisa's specific teaching. In contrast, it is clear from the claims that the claimed invention does not use such a resistance element, and the application further explains that the principle of the claimed configuration is that the well beneath the source ***substitutes for*** the use of a resistance element as used by Morihisa (see page 24, beginning at line 4). Therefore it is submitted that the claimed structures reflect an application of knowledge that is not provided by Morihisa, namely, that a well beneath the source can be used instead of a resistance element between the input terminal and the drain.

Accordingly it is believed that independent claims 1, 4 and 8 are distinguished on this basis. The remaining claims depend from claim 1, 4 or 8 and are distinguished for the reasons provided above as well as for the additional novel features recited therein.

The foregoing amendments and remarks address all bases for objection and rejection and are believed to place the case in condition for allowance. The examiner is invited to contact the undersigned to resolve any remaining issues.

Respectfully submitted,

By 

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yasuyuki MORISHITA
Title:	SEMICONDUCTOR DEVICE
Application No.:	09/621,614
Filing Date:	07/21/00
Examiner:	Nadav, Ori
Art Unit:	2811

VERSION SHOWING CHANGES MADE IN REPLY TO OFFICIAL ACTION OF 5 NOVEMBER 2002 UNDER 37 CFR §1.111

Commissioner for Patents
Box Non-Fee Amendment
Washington, D.C. 20231

Sir:

In reply to the official action mailed 5 November 2002, the application is amended as follows:

In the claims:

1. (Twice Amended) A semiconductor device having an input/output protection circuit section on a semiconductor substrate, ~~wherein~~the input/output protection circuit section comprising:

~~said input/output protection circuit section comprises~~ a plurality of field effect transistors connected in parallel, each of which has a ~~first~~ source diffusion layer of a first conductive type and a ~~second~~ drain diffusion layer of the first conductive type, and a gate electrode that is disposed between said ~~first~~ source and ~~second~~ drain diffusion layers; and

a dopant diffusion region of a second conductive type that is set at a distance from said plurality of field effect transistors~~,~~;

wherein said dopant diffusion region is connected to a reference potential, ~~and~~

wherein the ~~second~~ drain diffusion layer is connected directly to an input/output terminal section without an intervening resistance element~~,~~; and

wherein ~~under the first diffusion layer, there is formed~~ a first conductive type well ~~with~~ having a lower dopant concentration than the ~~first~~ source diffusion layer is formed under the source diffusion layer.

2. (Twice Amended) The semiconductor device according to Claim 1, wherein said gate electrode and said dopant diffusion region of the second conductive type are disposed over a second conductive type well that is formed on the surface of the semiconductor substrate~~,~~; and

wherein the bottom of said first conductive type well is formed at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well.

3. (Amended) The semiconductor device according to Claim 1, wherein said plurality of field effect transistors are N-channel type field effect transistors.

4. (Twice Amended) A semiconductor device having, on a semiconductor substrate, an input/output protection circuit section, the input/output protection circuit section comprising ~~that contains a complementary field effect transistor, wherein:~~

~~said~~ a complementary field effect transistor ~~comprises~~ including a first field effect transistor having a ~~first~~ source diffusion layer of a first conductive type, a ~~second~~ drain diffusion layer of the first conductive type, and a gate electrode that is disposed between ~~these~~ source and drain diffusion layers of the first conductive type, and a second field effect transistor having a ~~third~~ source diffusion layer of a second conductive type, a ~~fourth~~ drain diffusion layer of the

second conductive type, and a gate electrode that is disposed between ~~these~~ source and drain diffusion layers of the second conductive type,~~;~~

wherein a first dopant diffusion region of the second conductive type is set at a distance from said first field effect transistor, and a second dopant diffusion region of the first conductive type is set at a distance from said second field effect transistor~~;~~,

wherein the first dopant diffusion region is connected to a first reference potential, the second dopant diffusion region is connected to a second reference potential, ~~and~~

wherein the ~~second~~ drain diffusion layer of the first field effect transistor and the ~~fourth~~ drain diffusion layer of the second field effect transistor are each connected directly to an input/output terminal section without an intervening resistance element,~~;~~ and

wherein under the ~~first~~ source diffusion layer of the first field effect transistor~~,~~ there is formed a first conductive type well ~~with~~ having a lower dopant concentration than the ~~first~~ source diffusion layer of the first field effect transistor.

5. (Twice Amended) The semiconductor device according to Claim 4, wherein the gate electrode of the first field effect transistor and the first dopant diffusion region are disposed over a second conductive type well that is formed on the surface of the semiconductor substrate~~;~~, and

wherein the bottom of said first conductive type well is formed at the same depth as the bottom of the second conductive type well or at a level deeper than the bottom of the second conductive type well.

6. (Twice Amended) The semiconductor device according to Claim 5, wherein, beneath the second conductive type well, there is set a dopant high-concentration region containing second conductive type dopants with a higher dopant concentration than the second conductive type well~~;~~, and

wherein the bottom of said first conductive type well is formed at the same depth as the bottom of said dopant high-concentration region or at a level deeper than the bottom of said dopant high-concentration region.

7. (Amended) The semiconductor device according to Claim 4, wherein the first field effect transistor is an N-channel type field effect transistor.

8. (Amended) A semiconductor device having an input/output protection circuit section on a semiconductor substrate, the input/output protection circuit section comprising~~wherein~~:

~~said input/output protection circuit section comprises~~ a plurality of field effect transistors connected in parallel, each of which has a ~~first~~ source diffusion layer of a first conductive type and a ~~second~~ drain diffusion layer of the first conductive type and a gate electrode that is disposed between said first and second diffusion layers; and

a dopant diffusion region of a second conductive type that is set at a distance from said plurality of field effect transistors,~~;~~

wherein said dopant diffusion region is connected to a reference potential, ~~and~~

wherein the ~~second~~ drain diffusion layer is connected directly to an input/output terminal section without an intervening resistance element,~~;~~

wherein ~~under the first diffusion layer, there is formed~~ a first conductive type well with a lower dopant concentration than the source ~~first~~ diffusion layer is formed under the source diffusion layer,~~;~~ and

wherein the first conductive type well at least partially underlies an element isolation film separating the source diffusion area from the dopant diffusion region of the second conductive type.